URSI GASS 2021, Rome, Italy, 28 August - 4 September 2021

SIW-based Multilayer GCPW-to-Dielectric Waveguide Transition in PCB technology at V-Band

Thanh-Luan Vu[(1)],[(2)], Jean Razafiarivelo[(2)], Ronan Sauleau[(1)], David González-Ovejero[(1)] and Mauro Ettorre[(1)]
(1) Univ Rennes, CNRS, IETR (Institut d'électronique et des technologies du numérique) - UMR 6164, 35000 Rennes, France
(2) APTIV France Company, 28230 Épernon, France

Abstract

This paper describes the design of a novel multilayer transition from a Grounded Coplanar Waveguide (GCPW) to a dielectric waveguide (DWG) at V-band. The key component of the transition is a stepped transformer using Substrate Integrated Waveguide (SIW) technology. The proposed transformer consists of a 5-layer stack-up, it is well-suited for Printed Circuit Board (PCB) fabrication process, and provides high coupling between the GCPW and the DWG at the edge of the PCB. The performance of the proposed transition has been analyzed by full-wave simulations for a transition connecting a GCPW line to a PTFE circular waveguide with a core diameter of 3.06 mm. Simulated results show an insertion loss under 0.84 dB and an input reflection coefficient better than -20 dB over the entire V-band.

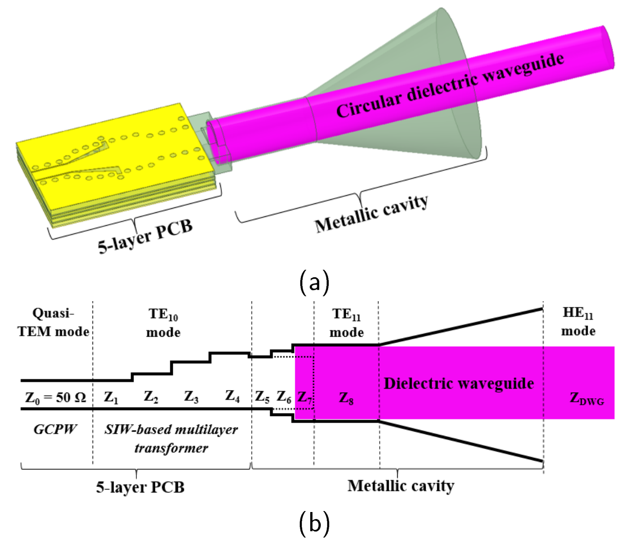
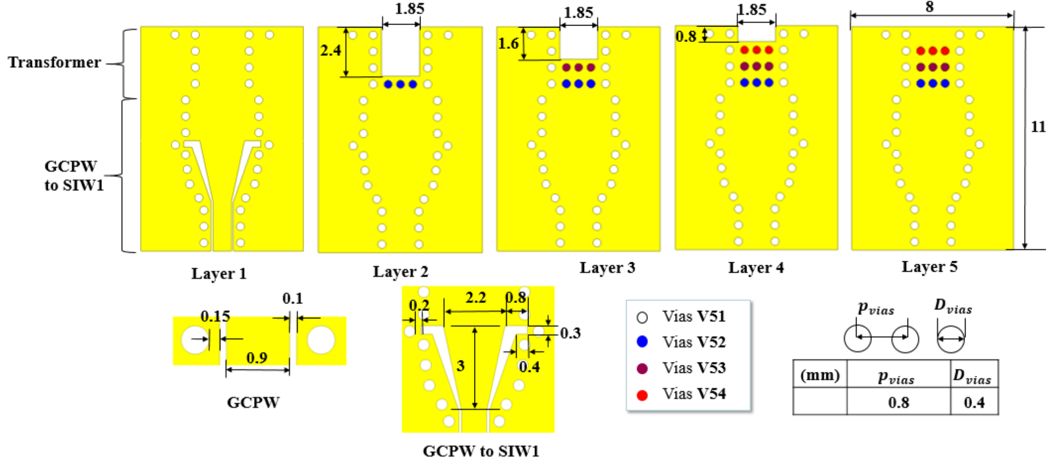


Figure 1. GCPW-to-DWG transtion, (a) 3D view and (b) cross-section

1 Introduction

Dielectric waveguides are an upward trend in replacing copper cables and optical fibers for multi-gigabit data communication systems at millimeter waves [1-3]. Ultra-high speed wired links use radio-frequency integrated circuits (RFICs) with CMOS technology and mm-wave DWGs as transmission channels. The interconnect between the RFICs and the DWGs can be one of the "bottlenecks" of the link [4]. To avoid this issue, vertical transitions from the top face of the chip to the DWG have been proposed in [3, 5]. Such configurations may be mechanically unstable for some applications, like automotive ones. Conversely, horizontal transitions represent an effective and more mechanically robust solution. The authors of [6] proposed a dipole to connect the chip to the DWG obtaining a measured insertion loss between 2.5 and 5 dB in the 60 - 67 GHz frequency range. A tapered slot antenna was proposed in [7] for chip-to-DWG coupler with a measured insertion loss between 3.4 and 6 dB in the 100 - 140 GHz band. The main drawback of two latter configurations were the significant radiation losses. On the other hand, [8] proposed a broadband CPW-to-rectangular DWG interconnect consisting of two sections: a CPW-to-ridged rectangular waveguide transition and a transition between the ridged waveguide and the DWG at D-band. The rectangular DWG in [8] had a tapered tip end which is not suitable in real applications due to its low tolerance to external forces. In addition, a misalignment between the CPW and the ridged waveguide and an asymmetry of the tapered tip degraded the performance of such configuration, which shows a measured insertion loss between 2 to 4.5 dB over the entire D-band. In general, the chip-to-DWG interconnect requires low-loss coupling, good mechanical robustness and compatibility with to classical RF components (e.g. connectors) for the mm-wave wired links. Substrate Integrated Waveguide (SIW) is a promising and low-cost technology for such interconnects [9]. In this paper, we present the design of a novel SIW-based transition from GCPW to circular DWG in multilayer PCB technology at V-band. The proposed transition consists of a SIW-based stepped transformer, which uses a 5-layer PCB stack-up to convert the electromagnetic waves from the GCPW to the DWG. Owing to the SIW-based stepped transformer, the proposed transition presents an estimated insertion loss lower than 0.84 dB from 50 to 75 GHz. Moreover, this transition can improve mechanical robustness and presents a good compatibility with integrated circuits.

This paper is organized as follow: section 2 describes the design of the proposed transition and section 3 presents the simulation setup and new paragraph results. Finally, conclusions are drawn in section 4.



(mm)	p_{vias}	D_{vias}
	0.8	0.4

Figure 2. Details of the layers and vias of the multilayer PCB stack-up

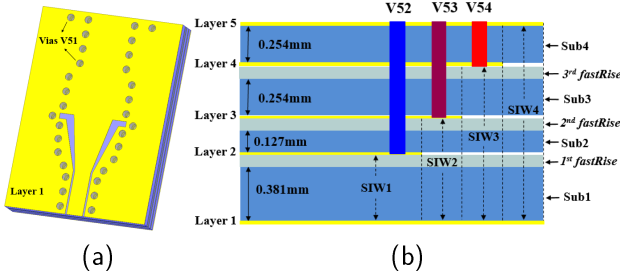


Figure 3. Multilayer PCB stack-up, (a) 3D view and (b) cross-section

2 Transition design

Fig. 1 shows a 3D view and the cross-section of the proposed transition. The transition consists of three parts: multilayer PCB stack-up, metallic cavity and DWG. The transition must transform from the quasi-TEM (transverse electromagnetic) mode of the GCPW to the fundamental HE_{11} (hybrid electromagnetic) mode of the DWG and, at the same time, must provide a good matching and acceptable loss in the band of interest (see Fig. 1b). The quasi-TEM mode of the GCPW is transformed to the HE_{11} mode of the DWG through two intermediate modes: the TE_{10} (transverse electric) mode of the SIW and the TE_{11} mode of the dielectric loaded waveguide. The impedance matching between the GCPW line (Z_0 = 50 Ω) and the DWG (Z_{DWG}) is achieved by a multisection stepped SIW-based transformer in PCB technology.

A. Multilayer PCB stack-up

In turn, the PCB stack-up can be splitted in two parts: a GCPW-to-SIW line (SIW1) transition and a multisection stepped SIW-based transformer. The GCPW-to-SIW1 transition is 3 mm long (see Fig. 2) and is located in substrate 1 between layers 1 and 2. This transition transforms the quasi-TEM mode in the GCPW to the TE_{10} mode in SIW1. The next part is a multisection stepped transformer from SIW1 to SIW4 (see Fig. 3). The dominant mode TE_{10} in SIW1 is converted to the TE_{10} in SIW4 by the intermediate steps SIW1-to-SIW2, SIW2-to-SIW3 and SIW3-to-SIW4 each 0.8 mm long. Vias V52, V53 and V54 reduce unexpected radiation losses during the transformations. Finally, the mode TE_{10} in SIW4 feeds the metallic cavity at the edge of the PCB stack-up.

The PCB stack-up of the proposed transition consists of five copper layers with thickness 17.5 μm, as shown in Fig. 2. The stack-up is made of four Roger RT/duroid 5880 substrates (ε_r = 2.2, tanδ = 0.0009 at 10 GHz) with thickness 0.381 mm, 0.127 mm, 0.254 mm and 0.254 mm (see Fig. 3). Each substrate is glued with fastRise (ε_r = 2.7, tanδ = 0.0017 and 0.076 mm thickness). The multilayers PCB requires four groups of vias V51, V52, V53 and V54 connecting layer 5 to layer 1, layer 2, layer 3 and layer 4, respectively. All vias must be metallized. Vias V51 provide side walls of the structure and V52, V53 and V54 prevent leakage. The 50 Ω GCPW with a width of 0.9 mm and 0.1 mm gap is etched on layer 1 while layer 2 is a ground plane. Layer 2, layer 3 and layer 4 present a slot for coupling the various stages (see Fig. 2). The width of the slots on layer 2, 3 and 4 is 1.85 mm and their lengths are 2.4, 1.6 and 0.8 mm, respectively. With this setup, four SIW lines are formed between layers 1 - 2 (SIW1), layers 1 – 3 (SIW2), layers 1 – 4 (SIW3) and layers 1 – 5 (SIW4) (see Fig. 3b).

B. Metallic cavity

The metallic cavity connecting the edge of the multilayer PCB to the DWG can be divided into two parts, as shown in Fig. 4. The first section includes a rectangular box with dimension of 5 × 1.5 × 1.3 mm^3 fed by the TE_{10} mode of SIW4. After the rectangular box, one finds the cylindrical cavities C1 and C2 (with 2.3 and 3.06 mm diameters, respectively), with the DWG inserted into C2. This section transforms the TE_{10} mode in SIW4 to the TE_{11} mode in the dielectric loaded circular waveguide. Finally, the conical section after C2 converts the TE_{11} mode to the HE_{11} mode of the DWG.

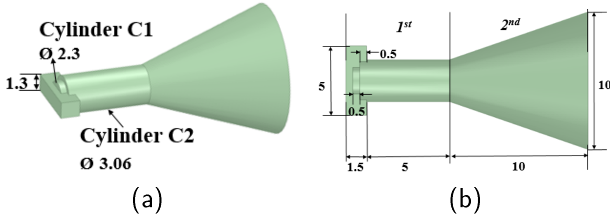


Figure 4. Metallic cavity, (a) 3D view and (b) cross-section

C. Dielectric waveguide

In this study, we selected a circular solid DWG from Polyfluor Plastics BV. The DWG presents a diameter of 3.06 mm and is made of PTFE with $\varepsilon_r = 2.03$, $\tan\delta = 0.0003$ at V-band. The chosen waveguide is mono-modal in the band of interest. Fig. 5 depicts the simulated and measured losses of the considered DWG at V-band. The average attenuation of the DWG is about 1.7 dB/m.

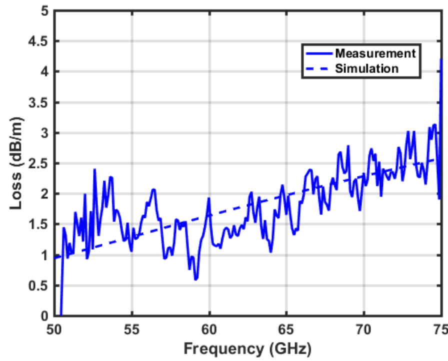


Figure 5. Simulated and measured loss of the DWG

3 Simulation results

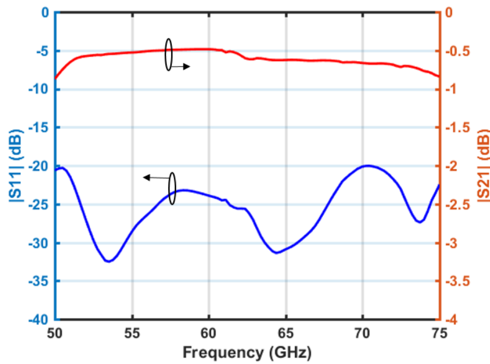


Figure 6. Simulated S-parameters of the proposed transition

The proposed transition has been simulated by Ansys HFSS [10]. In the simulation setup, a solid circular DWG 25.5 mm long is considered in the metallic cavity of the transtion. In addition, the $\tan\delta$ value of the Roger RT/duroid 5880 substrates are considered equal to 0.002 at 60 GHz as estimated during measurements in [11]. Fig. 6 represents the simulated magnitudes of the reflection and transmission coefficients. During simulations, the input reflection coefficient is less than -20 dB and the insertion loss is lower than 0.88 dB at V-band. Note that in this simulation the total transition loss and the attenuation of the DWG with length of 25.5 mm are included in these values. Thus, the extracted insertion loss of the proposed transition is less than 0.84 dB.

4 Conclusion

In this paper, we have described a transition from the GCPW to the circular DWG by using a SIW-based transformer in multilayer PCB technology. The proposed transition presents promising performances with losses estimated lower than 0.84 dB from 50 GHz to 75 GHz. The transition also presents good mechanical robustness. In addition, the SIW-based transformer can be compatible with integrated components in high-speed communication links at millimeter waves. The transition is currently under fabrication for testing in the coming months.

References

[1] M. De Wit, S. Ooms, B. Philippe, Y. Zhang and P. Reynaert, "Polymer microwave fibers: a new approach that blends wireline, optical, and wireless communication," *IEEE Microw. Mag.*, vol. 21, no. 1, pp. 51-66, Jan. 2020.

[2] J. Y. Lee, H. I. Song, S. W. Kwon, and H. M. Bae, "Future of highspeed short-reach interconnects using clad-dielectric waveguide," *Proc. SPIE*, vol. 10109, Feb. 2017, Art. no. 1010903.

[3] N. Van Thienen, W. Volkaerts and P. Reynaert, "A multi-gigabit CPFSK polymer microwave fiber communication link in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1952-1958, Aug. 2016.

[4] J. W. Holloway, G. C. Dogiamis and R. Han, "Innovations in terahertz interconnects: high-speed data transport over fully electrical terahertz waveguide links," *IEEE Microw. Mag.*, vol. 21, no. 1, pp. 35-50, Jan. 2020.

[5] U. Dey and J. Hesselbarth, "Millimeter-wave chip-to-chip interconnect using plastic wire operating in single and dual mode," *Proc. 2018 IEEE/MTT-S Int. Microw. Sym. (IMS)*, Philadelphia, PA, 2018.

[6] N. Dolatsha et al., "Fully-packaged mm-wave dielectric waveguide with multimode excitation," Electron. Lett., vol. 51, no. 17, pp. 1339-1341, 2015.

[7] N. Van Thienen, P. Reynaert, Y. Zhang, and M. De Wit, "An 18 Gbps polymer microwave fiber (PMF) communication link in 40 nm CMOS," in Proc. ESSCIRC Conf. 2016: 42nd European Solid-State Circuits Conf., pp. 483–486.

[8] W. Tsai et al., “Novel broadband transition for rectangular dielectric waveguide to planar circuit board at D band,” *IEEE MTT-S Int. Microw. Sym. (IMS)*, Philadelphia, PA, 2018.

[9] D. Deslandes and K. Wu, “Integrated microstrip and rectangular wave-guide in planar form,” *IEEE Microw. Wirel. Compon. Lett.*, vol. 11, no. 2, pp. 68–70, Feb. 2001.

[10] ANSYS Inc., “HFSS, Version 19,” Pittsburgh, PA, 2019.

[11] Y. Li and K. Luk, “60-GHz substrate integrated waveguide fed cavity-backed aperture-coupled microstrip patch antenna arrays,” *IEEE Trans. on Antennas and Propag.*, vol. 63, no. 3, pp. 1075-1085, March 2015.