# Efficiency Improvement of Power Amplifiers without Degraded Linearity Using a New Topology and Control Method

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## Abstract

This paper presents a medium-power amplifier designed in class AB at 2.4 GHz with two transistors of the same type in parallel. Keeping the drain bias of the transistors constant, it is demonstrated that by careful selection of the transistor and dynamically tuning the gate bias of the individual devices and output matching of the whole amplifier according to input drive level, an increase of about 40% in PAE is achieved at 7 dB back-off from the P1dB of the class AB amplifier employing a fixed bias and matching network and giving the same maximum output power. On the other hand, at higher drive levels while maintaining the PAE nearly constant (the same situation that is experienced in Doherty techniques), a maximum improvement of 7 dB can be observed at 1 dB compression point.

## 1. Introduction

The linearity of class-A and class-AB amplifiers are good for power amplifier applications, but the power efficiencies of these two types are poor. If the bias point can dynamically vary in a class-AB amplifier according to the varying envelope of the incoming RF input signal, power can be saved significantly [1].

Moreover, dynamic load modulation is one of the techniques that can be used to boost the PA efficiency when a variable envelope modulated signal is used [2]. Using load-line theory one can show that in a PA, maximum possible power can be delivered to the load over the input drive variation if the load impedance presented to the transistor is adjusted to the optimal value (optimum Cripps load) according to the input power level [3].

In this study, a mixture of both variable bias and tunable matching concepts is applied in an amplifier with two transistors in parallel. Utilizing a two-tone load-pull analysis, a novel computer aided design methodology based on [4] has been proposed for careful selection of the biasing points of the individual transistors in order to generate local intermodulation distortion (IMD) minimums or sweet spots.

## 2. Design Methodology

When a true transistor package with a realistic model and parasitics is to be used in a design, we have to deal with a lot of feedback elements. These components ultimately makes the de-embedding process and finding the closed form expressions for the proper bias range and complex load impedances which delivers the maximum power to the load a tedious task or even impossible, demanding inevitably a computer aided design method.

The design procedure in this work is composed of two-tone load-pull analysis of the amplifier with two sweeping parameters and determining the proper transistor type and gate bias range, followed by specifying the desired load impedance trajectory, and finally designing the tunable matching network. The schematic of the PA is shown in Fig. 1 where the tunability of the matching networks is presented by the variable capacitors.

## 2.1 Load-Pull Analysis

The active device being used in our work is ATF-50189, an enhancement mode pHEMT from Agilent which has been selected form a couple of choices due to the presentation of a proper behavior of third order IMD while sweeping $V_{GS}$ and input power which is going to be clarified in the following. First, one of the transistors is biased at $V_{GS2}$ = 0.2 V for a class-AB operation and $V_{GS}$ of the other device is swept from nearly cut-off towards the maximum allowed value close to the saturation region ($V_{GS1}$ = 0.15 V to 0.7 V). The drain bias for both of the transistors is chosen a typical value of $V_{DS}$ = 4.5 V. Primarily, one-tone load-pull simulation was performed at the center frequency of 2.4 GHz using the transistor model provided by the foundry in Agilent ADS.

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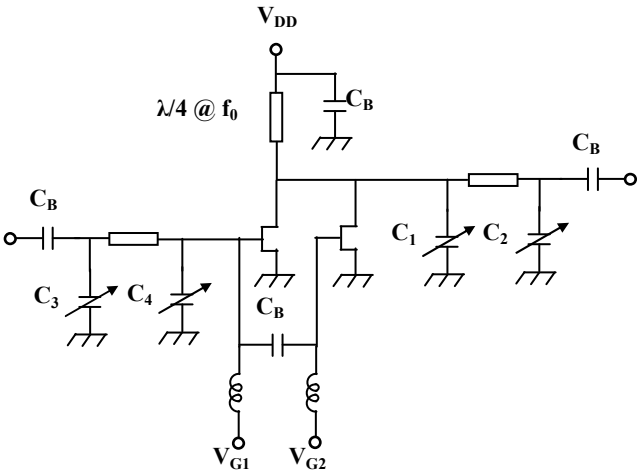


Fig. 1. Simplified schematic of the PA with tunable input and output matching networks.

Hence the load-pull circles and specifically the location of the load impedances for maximum output power at the fundamental frequency for different values of $V_{GS1}$ is obtained. A second parameter was also swept during the prescribed load-pull simulation which is the input power of the amplifier. In this way, a set of load impedances for different values of $V_{GS1}$ and driving power is attained as shown for three values of $V_{GS1}$ in Fig. 2.

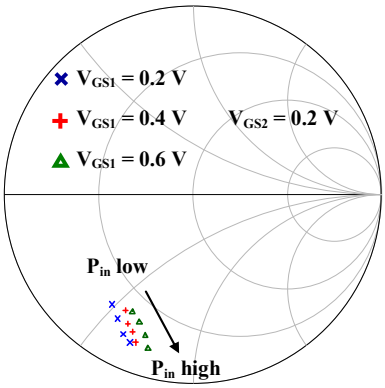


Fig. 2. Load impedance trajectory as $P_{in}$ increases for different $V_{GS1}$ values

Subsequently, a two-tone load-pull simulation was also performed at the center frequency of 2.4 GHz with a frequency spacing of 1 MHz between two tones in order to obtain the IMD behavior. For any value of the load impedance derived previously, the third order IMD pattern can be plotted versus $V_{GS1}$ while $P_{in}$ is swept as a parameter on the figure. One such a plot is presented in Fig. 3 for one of the arbitrary impedance points $Z_L$ = 9.2 - j 30.5.

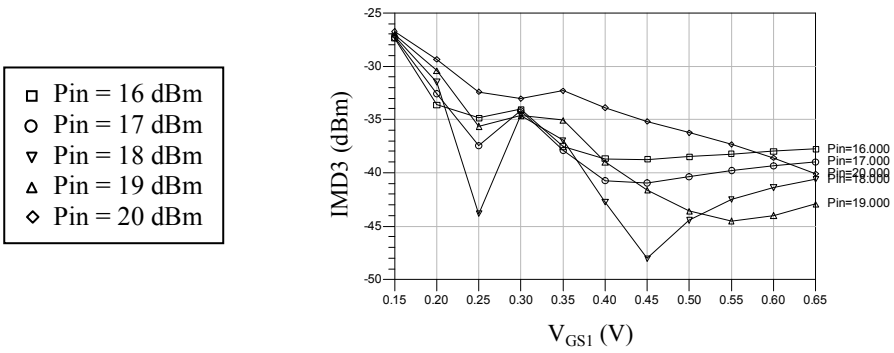


Fig. 3. Third order IMD as a function of $V_{GS1}$ and $P_{in}$ for $V_{GS2}$=0.2 V

As can be seen, for the $P_{in}$ values less than 16 dBm there is an increasing trend in IMD3 with input power as expected but as $P_{in}$ expands beyond 16 dBm, intermodulation level starts to decrease for all the $V_{GS1}$ values greater than 0.2 V and then a sudden rise can be observed at $P_{in}$ = 20 dBm. This kind of behaviour actually predicts the existence of a large signal sweet spot for the given $V_{GS}$ values. The presence of sweet spots is the main factor in lowering the intermodulation at higher drive levels. On the other hand, occurrence of minimum spot in IMD3 results in a small ripple on the power gain plot as shown in the results section. This is the main fact that has been utilized in a parallel device structure for the first time in this paper in order to improve the 1dB compression points at higher drive levels.

## 2.2 Bias and Load Selection

The main idea behind the selection of the gate bias and load values is the fact that in the first place the output $P_{1dB}$ of the amplifier increases at higher input drive levels if being adjusted to the optimum Cripps load which in turn follows the traces illustrated in Fig. 2. On the other hand, as the load impedance increases, the efficiency peak moves from high power to low power region, thus enhancing the efficiency at reduced drive levels. The same situation prevails when changing the gate bias. Namely, with increasing the gate voltage of one of the transistors, the output $P_{1dB}$ point improves while the efficiency peak shifts to high power values.

Making use of both of these facts, a combinational set of $V_{GS}$ for individual devices and load impedances can be judiciously chosen among a bunch of choices which allows a continuous rise of the output $P_{1dB}$ with increasing the input power together with a nearly constant power added efficiency. This is while the efficiency is enhanced for the reduced drive levels with keeping the biases at the lowest possible values and designing the output matching at low input power region. Each combination of $V_{GS1}$, $V_{GS2}$ and load impedance can be considered to be a 'state' in which the amplifier operates according to the input signal level. TABLE I summarize the 7 different states that the amplifier switch in between.

Table 1. Seven Operational States of the Amplifier

| $V_{GS1}$ (V) | $V_{GS2}$ (V) | $Z_L$ (Ω) | $P_{1dB}$ (dBm) |
|---|---|---|---|
| 0.2 | 0.2 | 10 - j 24.5 | 28.8 |
| 0.2 | 0.2 | 9 – j 27.6 | 29.9 |
| 0.3 | 0.2 | 8.8 – j 29.7 | 30.8 |
| 0.5 | 0.2 | 10.8 – j 30 | 31.5 |
| 0.5 | 0.2 | 8.6 – j 31.9 | 32.8 |
| 0.5 | 0.2 | 6.3 – j 33.8 | 34.2 |
| 0.6 | 0.3 | 5.6 – j 35.8 | 36.0 |

It can be seen that along with changing the complex optimum load impedance together with the gate bias voltages, an improvement in the output 1dB compression point from 28.8 dBm to 36.0 dBm for the first amplifier and from 30.5 dBm to 35.6 dBm for the second one is attained. This is while the PAE after reaching its peak value at the first state is tried to experience small drops in transition between states as will be shown later. Ideally, at the terminal of the transistor current source, the desired load impedance is purely real; however, at the external terminal of the transistor, the desired load trajectory deviates from the real axis due to the drain-to-source capacitance, bond-wire inductance, and package parasitic effects [5].

## 2.3 Tunable Matching Network

The most suitable topology for the tunable matching network in our design can be a Π network with two tunable capacitors and a fixed transmission line between them as presented in Fig. 1. It was chosen due to its simplicity in tuning and low Q. For our designs the shunt capacitance values ranging from 1 pF to 10 pF and the fixed transmission line of L = 15 mm and W = 2 mm on the Rogers substrate RO4003C was chosen which corresponds to the characteristic impedance of $Z_0$ = 47 Ω and electrical length of 73° at the design frequency. These values can well span the desired impedance area on the smith chart.

## 3. Nonlinear Analysis Results

Fig. 4 and Fig. 5 display the PAE and the gain at 7 operational states of the amplifier, respectively. As can be seen, PAE is kept constant at average value of about 52 % from the output power of 29 dBm to 36 dBm where it starts to drop.

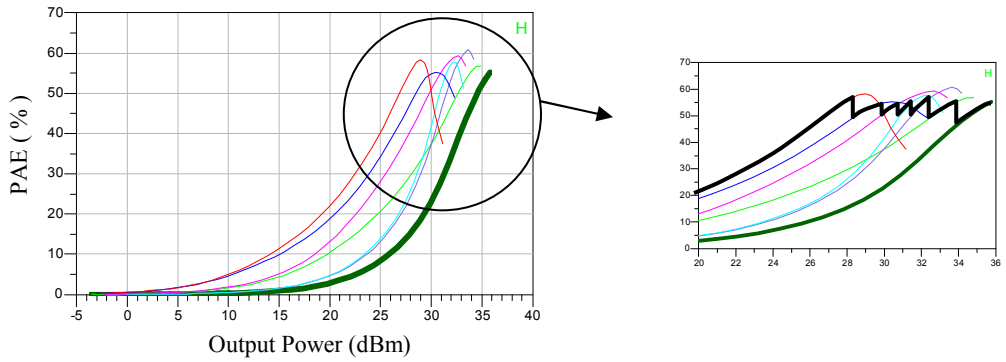


Fig. 4. Power added efficiency at 7 operational states from the lowest $P_{1dB}$ on the left most to the highest at the right most.

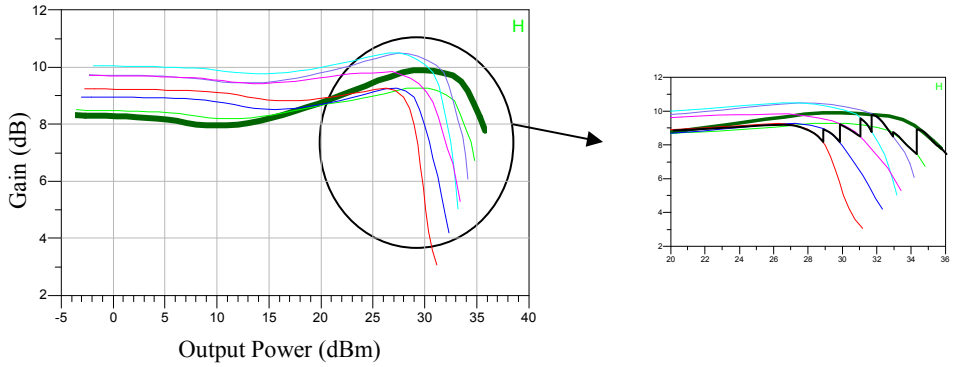


Fig. 5. Power gain of the amplifier at 7 operational states from the lowest $P_{1dB}$ on the left most to the highest at the right most.

## 4. Acknowledgments

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## 5. References

1. K. Yang, J. R. East, and G. I. Haddad, "Automatic control of efficiency and linearity in power amplifiers for low-power wireless communication," *1998 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems. Dig.*, September 1998, pp. 113-118.

2. H. M. Nemati, C. Fager, U. Gustavsson, R. Jos, and H. Zirath, "Design of varactor-based tunable matching networks for dynamic load modulation of high power amplifiers," *IEEE Trans. Microwave Theory & Tech.*, vol. 57, no. 5, May 2009, pp. 1110-1118.

3. S. C. Cripps, *RF Power Amplifiers for Wireless Communications, Second Edition,* Boston, MA: Artech House, 2006.

4. N. B. Carvalho, J. A. Garcia, E. Azpitarte, and J. C. Pedro, "Load-impedance selection for maximized large signal IMD sweet-spot effects," *International Journal of RF and Microwave Computer-Aided Engineering,* vol. 15, issue 5, September 2005, pp. 434-440.

5. J. Shiang Fu, and A. Mortazawi, "Improving power amplifier efficiency and linearity using a dynamically controlled tunable matching network," *IEEE Trans. Microwave Theory & Tech.,* vol. 56, no. 12, December 2008, pp. 3239-3244.